Amendments to the Specification

Please replace paragraph [0001] under the heading **TECHNICAL FIELD OF THE INVENTION** ***with the following amended paragraph:***

The present invention relates to a system [[LSI]] large scale integration (LSI) including a plurality of circuit blocks. More particularly, the present invention relates to a system LSI designed to perform a test operation of circuit blocks for a shorter period of time.

Please replace paragraph [0020] with the following amended paragraph:

As described above, according to the second preferred embodiment, the total duration of test is "t1+t2+t3[[+t4]]".

Please replace paragraph [0021] with the following amended paragraph:

Figs. 5A and 5B are circuit (block) diagrams showing a system LSI according to a third embodiment of the present invention. The system LSI includes a plurality of circuit blocks IP1, IP2 and IP3, which are connected to first to third terminals vdd1, vdd2 and vdd3, respectively. All of the circuit blocks IP1 to IP3 are tested on a wafer before fabrication of the system LSI is completed. The circuit blocks IP1 to [[IP4]] IP3 may be a logic circuit, an analog circuit, a memory circuit, and so on. Fig. 5A illustrates the configuration on a wafer.

Please replace paragraph [0023] with the following amended paragraph:

As described above, according to the third preferred embodiment, the total duration of test becomes shorter as compared with the conventional technology. Since the circuit blocks IP1 to IP3 are tested individually and independently on the wafer, the total duration is determined based on the longest test period for a specific circuit block, IP1, IP2 or [[Ip3]] IP3.